

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: SAKAMOTO  
 Docket: 10233.81USW1  
 Title: SEMICONDUCTOR DEVICE AND A METHOD FOR MANUFACTURING THEREFOR

CERTIFICATE UNDER 37 CFR 1.10

'Express Mail' mailing label number: EL176165550US

Date of Deposit: November 25, 1998

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By:   
 Name: D. McGruder

BOX Patent Application  
 Assistant Commissioner for Patents  
 Washington, D.C. 20231

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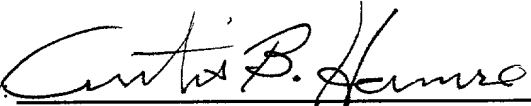
- ☒ Transmittal sheet, in duplicate, containing Certificate under 37 CFR 1.10.
- ☒ Utility Patent Application: Spec. 14 pgs; 8 claims; Abstract 1 pgs.  
 The fee has been calculated as shown below in the 'Claims as Filed' table.
- ☒ 10 sheets of formal drawings
- ☒ An unsigned Combined Declaration and Power of Attorney
- ☒ A check in the amount of \$760.00 to cover the Filing Fee
- ☒ Other: Preliminary Amendment; Submission of Priority Document
- ☒ Return postcard

**CLAIMS AS FILED**

Number of Claims Filed	In Excess of:	Number Extra	Rate	Fee
<b>Basic Filing Fee</b>				\$760.00
<b>Total Claims</b>				
8	20	0	x 0.00	\$0.00
<b>Independent Claims</b>				
3	3	0	x 0.00	\$0.00
<b>MULTIPLE DEPENDENT CLAIM FEE</b>				\$0.00
<b>TOTAL FILING FEE</b>				\$760.00

Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: SAKAMOTO Docket No.: 10233.81USW1  
Serial No.: Unknown Filed: Unknown  
Int'l Appln No.: PCT/JP98/01325 Int'l Filing Date: March 25, 1998  
Title: SEMICONDUCTOR DEVICE AND METHOD FOR  
MANUFACTURING THEREFOR

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By: 

Name: D. McGruder

PRELIMINARY AMENDMENT

Box Patent Application  
Assistant Commissioner for Patents  
Washington, D. C. 20231

Dear Sir:

In connection with the above-identified application filed herewith, please enter the following preliminary amendment:

IN THE SPECIFICATION

Please insert the following new paragraph after the title:

--This is a Continuation application of PCT Application No. PCT/JP98/01325,  
filed March 25, 1998.--

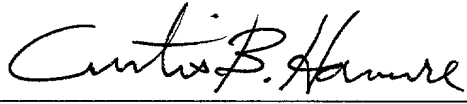
Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to calculation of the filing fee and prior to examination and consideration of the above-identified application.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicant's primary attorney-of record, Curtis B. Hamre (Reg. No. 29,165), at (612) 336-4722.

Respectfully submitted,

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Dated: November 25, 1998

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**[TITLE OF THE INVENTION]**

A Semiconductor Device and a Method for  
Manufacturing Thereof

**[Field of the Invention]**

The present invention relates to a  
5 semiconductor device, a part of which is irradiated by  
radiating rays, more specifically, a technology for  
radiating a part of the semiconductor.

**[Background art]**

An insulated gate bipolar transistor  
10 (hereinafter referred to as IGBT) 80 shown in Fig. 9 is  
known as a semiconductor device having a planar type high  
voltage-proof vertical element. The IGBT 80 is a  
semiconductor device which has both a high input  
impedance characteristic observed in a metal oxide field  
15 effect transistor (hereinafter referred to as MOSFET) and  
a low saturation voltage characteristic known as a  
characteristic of a bipolar transistor.

A substrate 82 used for the IGBT 80 includes a  
drain layer 3 with  $P^+$  type, an  $n^+$  type layer 5 and an  $n^-$   
20 type layer 7. Base regions 21 are formed in the  $n^-$  type  
layer 7, and source regions 23 with  $n^+$  type are formed  
within the base regions 21. Surface of the  $n^-$  type  
semiconductor layer 82 is covered with a gate oxidation  
layer 17.

25 Incidentally, a loss caused by switching arises

as a result of a parasitic diode generated on a plane of a PN (positive-negative) junction 59. Japanese Patent laid-open publication No. Hei 7-135214 discloses a technology for selectively radiating electron-beams using a mask 41 shown in Fig. 9 during the manufacturing processes in order to avoid the generation of the parasitic diode. The beams pass through through-holes 43 formed in the mask 41 and irradiated on the IGBT 80. In this way, the life-time of carriers located on the plane of the PN junction 59 where the parasitic diode being generated can be shorten as a result of forming crystal defects 61.

In the manufacturing processes described above, unexpected variation of the threshold voltage in the IGBT 90 is pointed out because of generation of bremsstrahlung caused by the material of the mask 41 made generally of a heavy metal such as lead and the like.

Japanese Patent laid-open publication No. Hei 8-227895 discloses another IGBT 90 having layers for restricting electron-beams. As shown in Fig. 10, a layer 69 for restricting the beams made of silicon nitride is formed under a source electrode where requiring restriction of the electron-beams. Generation of the bremsstrahlung is restricted even when the beams are radiated to the IGBT 90 under the condition due to masking of the restriction layer 69.

However, the number of process is increased because the processes for forming the restriction layers 69 made of silicon nitride is required in the conventional method.

5     **[Disclosure of the present invention]**

It is an object of the present invention to overcome the above mentioned drawbacks associated with prior arts, and to provide a semiconductor device and a method for manufacturing thereof capable of radiating  
10     electron-beams to the desired region with simple processes, while not providing adverse effects caused by bremsstrahlung even when the electron-beams are radiated.

In accordance with characteristics of the present invention, there is provided a semiconductor  
15     device comprises:

        a substrate having a region to be irradiated with radiating rays, and

        a metal wring layer located on the substrate one of directly and indirectly,

20     wherein the metal wring layer is made of a light metal,

        and wherein the metal wring layer located on the region to be irradiated is formed thinner than that formed on regions except for the region to be irradiated.

25     Also, in accordance with characteristics of the present invention, there is provided a semiconductor

device comprises:

a substrate having a region to be irradiated with radiating rays, and

5 a metal wiring layer located on the substrate, wherein the metal wiring layer is made of a light metal,

and the metal wiring layer is used as a mask for restricting penetration of the radiating rays into region except for the region to be irradiated.

10 Further, in accordance with characteristics of the present invention, there is provided a method for manufacturing a semiconductor device having a substrate, and a metal wiring layer located on the substrate, a region of the substrate being irradiated with radiating  
15 rays, the method comprises the steps of:

entirely forming the metal wiring layer, removing the metal wiring layer located on the region to be irradiated, and

20 radiating the radiating rays using the metal wiring layer being remained as a mask.

While the novel features of the invention are set forth in a general fashion, both as to organization and content, the invention will be better understood and appreciated, along with other objects and features  
25 thereof, from the following detailed description taken in conjunction with the drawings.

**[Brief description of the drawings]**

Fig. 1 is a sectional view showing part of an IGBT 1 as an embodiment of a semiconductor device in accordance with the present invention.

5 Fig. 2 is a perspective view of the IGBT 1.

Fig. 3 is a graph showing a relationship between a range of electrons in the source electrode 22 and energy amount of the electron-beams.

10 Fig. 4A through Fig. 4C are sectional views showing the manufacturing process of the IGBT 1.

Fig. 5A and Fig. 5B are another sectional views showing the manufacturing process of the IGBT 1.

Fig. 6A and Fig. 6B are far another sectional views showing the manufacturing process of the IGBT 1.

15 Fig. 7A and Fig. 7B are still another sectional views showing the manufacturing process of the IGBT 1.

Fig. 8 is yet another sectional view showing the manufacturing process of the IGBT 1.

20 Fig. 9 is a sectional view of the IGBT 80 in the conventional technology.

Fig. 10 is a sectional view of another IGBT 90 in the conventional technology.

**[The best mode of preferred embodiment to carry out the present invention]**

25 An embodiment of the present invention will be described herein with reference to the drawings. Fig. 1

is a sectional view showing part of an IGBT 1 as one embodiment of a semiconductor device in accordance with the present invention.

The IGBT 1 is formed in a substrate 2 for a semiconductor device. In the substrate 2, an  $n^+$  type layer 5 and an  $n^-$  type layer 7 are consecutively formed on a drain layer 3 with  $P^+$  type. A base region 21 with  $P^+$  type is formed in the  $n^-$  type layer 7. Source regions 23 are formed in the base region 21. The surface of the  $n^-$  type layer 7 is covered with a gate oxidation layer 15. A gate electrode 17 is formed on the gate oxidation layer 15. The gate electrode 17 is covered with an inter-insulating layer 19, and a source electrode 22 made of aluminum is formed on the inter-insulating layer 19. The source electrode 22 formed as a wiring layer made of a metal is also used for electrically connecting with the source regions 23 in the IGBT element. A passivation layer 29 covers entire surface of the source electrode 22. The first conductive type and the second conductive type are respectively defined as n type and p type in this embodiment.

A silicon oxidation layer 27 is formed on a region 24 located between the source regions 23 formed within the base regions 21. Further, the source electrode 22 is not existed at upper part of the silicon oxidation layer 27, and an opening 25 is located on the

silicon oxidation layer 27. On the other hand, a crystal defect region 11 is formed at a position in the  $n^-$  type layer 7 and below the silicon oxidation layers 27.

Fig. 2 is a perspective view of the IGBT 1 before forming the passivation layer 29. As described, the silicon oxidation layer 27 is formed above of the crystal defect region 11, and the opening 25 is located on the silicon oxidation layers 27. In this way, the source electrode 22 made of aluminum can be used both for a wiring, and a mask for the beams.

Next, a method for manufacturing the IGBT 1 will be described. The manufacturing processes similar to an ordinary IGBT are carried out until forming the source electrodes 23. In other words, the substrate 2 is formed by consecutively forming the  $n^+$  type layer 5 on the drain layer 3 and the  $n^-$  type layer 7 thereon as shown in Fig. 4A. Thereafter, the gate oxidation layer 15 and the gate electrode 17 are formed successively as shown in Fig. 4B. Ion implantation of P-type impurities is carried out by using the gate electrode 17 as a mask. Further, N-type impurities are implanted ionically by using both a resist layers 81 formed on the gate oxidation layer 15 and the gate oxidation layers 17 as a mask as shown in Fig. 4C. The base region 21 with  $P^+$  type and a pair of the source regions 23 located in the base region 21 are formed simultaneously by carrying out

thermal treatment as shown in Fig. 5A.

Next, a silicon oxidation ( $\text{SiO}_2$ ) layer 18 is accumulated entirely on the substrate with the chemical vapor deposition (CVD) method as shown in Fig. 5B. A resist layer 82 is formed above of both the crystal defect region 11 and the gate electrode 17 as shown in Fig. 6A. Both the inter-insulation layer 19 and the silicon oxidation layer 27 are formed with an etch-back technique by using the resist layers 82. In this way, the silicon oxidation layer 27 is formed above of the crystal defect region 11 as shown in Fig. 6B.

Next, aluminum is accumulated entirely on the substrate in thickness of 5  $\mu\text{m}$  with CVD method as shown in Fig. 7A.

As shown in Fig. 7B, the source region 22 is formed by carrying out etching using a resist layer 84 being formed. As a result of the etching, the opening 25 is formed on the silicon oxidation layer 27.

The crystal defect region 11 is irradiated by the electron-beams radiated from the above after removing the resist layer 84 as shown in Fig. 8. The radiation of the beams is carried out at 1 mega electro-volts in energy strength in this embodiment.

By carrying out the radiation, the crystal defect region 11 uncovered with the source electrode 22 is irradiated by the beams, so that desired crystal

defects are generated within the region 11. On the other hand, less amount of the beams are irradiated to regions existing outside of the region 11. Although, a certain amounts of crystal defects are generated in the regions existing the outside of the region 11, these defects can be removed by annealing carried out later. In this way, the IGBT 1 shown in Fig. 1 is manufactured.

Next, thickness of the source electrode 22 is described hereunder with reference to a relationship between a range of electrons in the source electrode 22 and energy amount of the beams. As shown in Fig. 3, the range of electrons in aluminum is increased when a higher energy is radiated. Usually, energy strength of the beams forming the crystal defect region is in a range from 600 electro-volts to 1 mega electro-volts. The source electrode 22 in thickness of 0.6 cm to 1 cm is required in order to restrict the generation of the crystal defect region with the source electrode 22 alone. However, the source electrode 22 relatively thicker than an ordinary aluminum wiring having a range from 1  $\mu\text{m}$  to 10  $\mu\text{m}$  is able to restrict the beams because the beams are restricted by the gate electrode 17, the passivation layer 19 and other layers formed thereunder.

Further, the generation of the bremsstrahlung caused by the source electrode 22 made of a heavy metal can be avoided even when the beams are directly radiated

to the source electrode 22 exposed to the air. Because the source electrode 22 is made of a light metal in this embodiment. In this way, only a desired region can be irradiated with the beams by using the source electrode made of aluminum capable of using both as a wiring and a mask for the beams as a result of making an opening at a region to be irradiated without forming a layer for restricting beams in addition to the layers described above.

Although, the beams are radiated after removing the resist layer 84, the radiation can be carried out without removing the resist layer 84.

Although, the present invention is applied to the IGBT in the embodiments described above, the present invention is also applicable to other types of semiconductors such as a power MOSFET transistor and the like used as a vertical type MOSFET. Further, the present invention can also be used in any semiconductor devices such as ordinary bipolar transistor or others as long as the semiconductor requires the radiation of the beams to a part of the substrate thereof.

Although, the source electrode 22 is made of aluminum, other light metals not causing bremsstrahlung such as an aluminum silicon and the like can be used for the source electrode 22. Any other metals not causing bremsstrahlung such as copper can be used for the source

electrode 22. Because of its higher density than that of aluminum, the use of copper allows the radiation of the beams to the desired region even when its profile is in a thin form. Further, tungsten can also be used for the source electrode 22.

Although, the IGBT is employed as a semiconductor having the region to be irradiated in the embodiment described above, the present invention can be applied to a semiconductor device having the IGBT.

Further, the silicon oxidation layer 27 is provided in order to form the opening 25 located above of the crystal defect region 11 in the embodiment. However, the opening can be formed directly on the source electrode 22 by carrying out etching thereto without providing the silicon oxidation layer.

The semiconductor device in accordance with the present invention is characterized in that, the metal wring layer is made of a light metal. Therefore, no generation of the bremsstrahlung is observed even when the radiation are radiated. Also, the metal wring layer located on the region to be irradiated is formed thinner than that formed on regions except for the region to be irradiated so as to reach the radiating rays to the region to be irradiated. In this way, the crystal defect region can only be formed in the desired region. As a result, it is possible to provide a semiconductor device

capable of radiating the radiating rays to the desired region with simple processes, while not providing adverse effects caused by bremsstrahlung even when the radiating rays are radiated. Also, the semiconductor device in accordance with the present invention is characterized in that, the metal wring layer located on the regions except for the region to be irradiated is formed in a thickness so as not to provide any adverse effect on the regions except for the region to be irradiated. Therefore, it is possible to avoid adverse effect on the regions except for the region to be irradiated.

Further, the semiconductor device in accordance with the present invention is characterized in that, the metal wring layer is made of a light metal, and the metal wring layer is used as a mask for restricting penetration of the radiating rays into region except for the region to be irradiated. Therefore, it is possible to provide a semiconductor device capable of radiating the radiating rays only to the desired region with simple processes, while not providing the adverse effects caused by bremsstrahlung even when the radiating rays are radiated.

The semiconductor device in accordance with the present invention is characterized in that, the semiconductor device is an insulated gate bipolar transistor (IGBT), and the region to be irradiated is a positive-negative junction region where a parasitic diode

is generated. Therefore, it is possible to provide an IGBT capable of overcoming a loss arising at the switching caused by generation of a parasitic diode.

Also, the semiconductor device in accordance with the present invention is characterized in that, the semiconductor device is a MOSFET, and the region to be irradiated is a positive-negative junction region where a parasitic diode is generated. Therefore, it is possible to provide a MOSFET capable of overcoming a loss arising at the switching caused by generation of a parasitic diode with a simple structure.

Further, the method for manufacturing a semiconductor device in accordance with the present invention is characterized in that, the method comprises the steps of entirely forming the metal wiring layer, removing the metal wiring layer located on the region to be irradiated, and radiating the radiating rays using the metal wiring layer being remained as a mask. Therefore, it is possible to provide a semiconductor device capable of radiating the radiating rays only to the desired region with simple processes without causing any adverse effects caused by the bremsstrahlung even when the radiating rays are radiated.

The semiconductor device in accordance with the present invention is characterized in that, the metal wiring layer is made of a metal which prevents the

generation of the bremsstrahlung even when the radiating rays are radiated, and the metal wring layer located on the region to be irradiated is formed thinner than that formed on regions except for the region to be irradiated so as to reach the radiating rays to the region to be irradiated. In this way, the crystal defect region can only be formed in the desired region. As a result, it is possible to provide a semiconductor device capable of radiating the radiating rays only to the desired region with simple processes, while not providing adverse effects caused by the bremsstrahlung even when the radiating rays are radiated.

While the invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather than limitation and that changes within the purview of the appended claims can be made without departing from the true scope and spirit of the invention in its broader aspects.

**What is claimed is:**

1. A semiconductor device comprising:

a substrate having a region to be irradiated with radiating rays, and

5 a metal wring layer located on the substrate one of directly and indirectly,

wherein the metal wring layer is made of a light metal,

10 and wherein the metal wring layer located on the region to be irradiated with radiating rays is formed thinner than that formed on regions except for the region to be irradiated so as to reach the radiating rays to the region to be irradiated.

15 2. The semiconductor device in accordance with claim 1, wherein none of the metal wring layer is located on the region to be irradiated.

20 3. The semiconductor device in accordance with claim 2, wherein an insulation layer is located on the region to be irradiated.

25 4. The semiconductor device in accordance with claim 3, wherein the metal wring layer located on the regions except for the region to be irradiated is formed in a thickness so as not to provide any adverse effect on

the regions except for the region to be irradiated.

5. A semiconductor device comprising:

a substrate having a region to be irradiated

5 with radiating rays, and

a metal wiring layer located on the substrate,

wherein the metal wiring layer is made of a

light metal,

and the metal wiring layer is used as a mask for

10 restricting penetration of the radiating rays into  
regions except for the region to be irradiated.

6. The semiconductor device in accordance with

claim 5, the semiconductor device is an insulated gate

15 bipolar transistor, and wherein the region to be

irradiated is a positive-negative junction region where a  
parasitic diode is generated.

7. The semiconductor device in accordance with

20 claim 5, wherein the semiconductor device is a metal

oxide semiconductor field effect transistor, and wherein

the region to be irradiated is a positive-negative

junction region where a parasitic diode is generated.

25 8. A method for manufacturing a semiconductor

device having a substrate, and a metal wiring layer

located on the substrate, a region of the substrate being irradiated with radiating rays, the method comprising the steps of:

- entirely forming the metal wiring layer,
- 5 removing the metal wiring layer located on the region to be irradiated, and
- radiating the radiating rays using the metal wiring layer being remained as a mask.

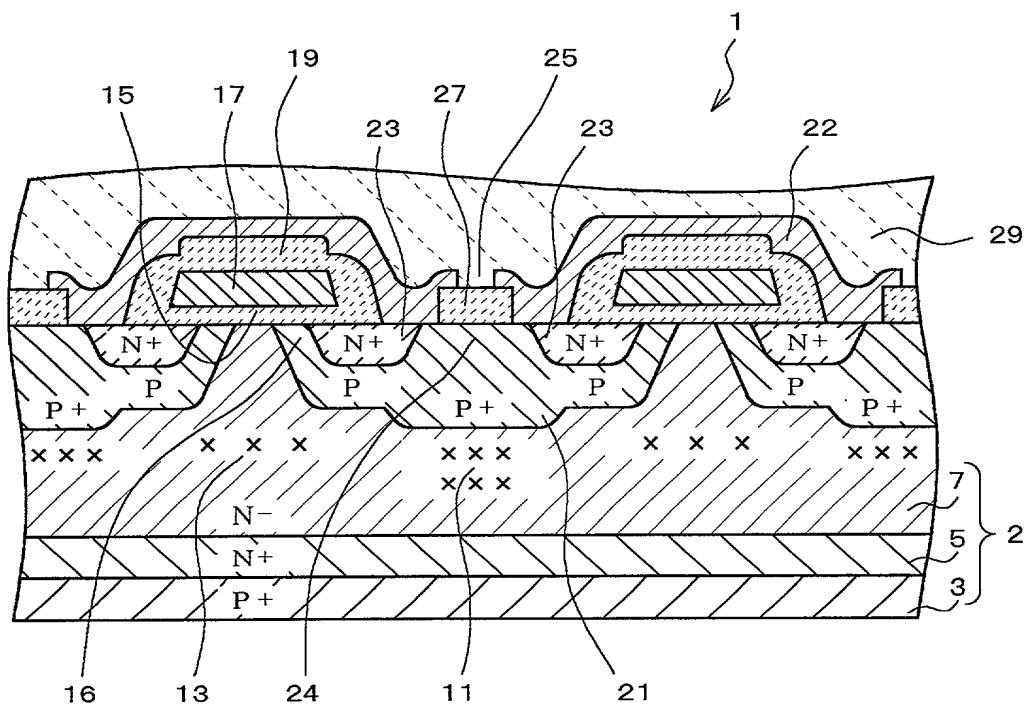
SECRET

**Abstract of Disclosure**

An object of the present invention is to provide a semiconductor device capable of radiating electron-beams only to a desired region without forming a layer for restricting the radiating rays. A source electrode 22 made of aluminum prevents the generation of bremsstrahlung even when the electron-beams are radiated to the source electrode in a exposed condition. Also, the source electrode having an opening 25 at above of a crystal defect region 11 is used as a mask when the electron-beams are radiated thereto. That is the source electrode made of aluminum can be used both as a wiring and a mask for the radiating rays.

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D. McCorader  
MSG/uder

FIG.1



**FIG.2**

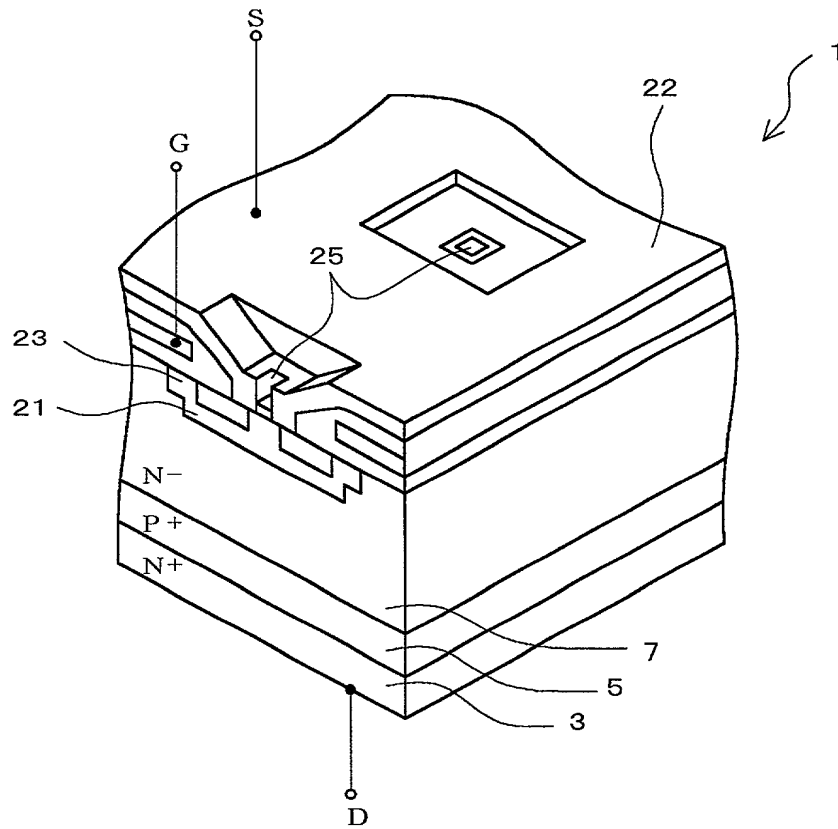


FIG.3

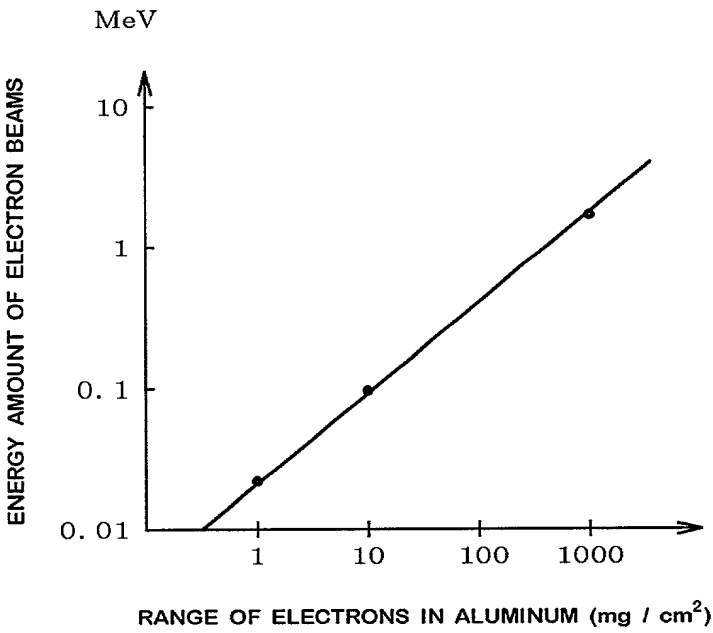


FIG.4A

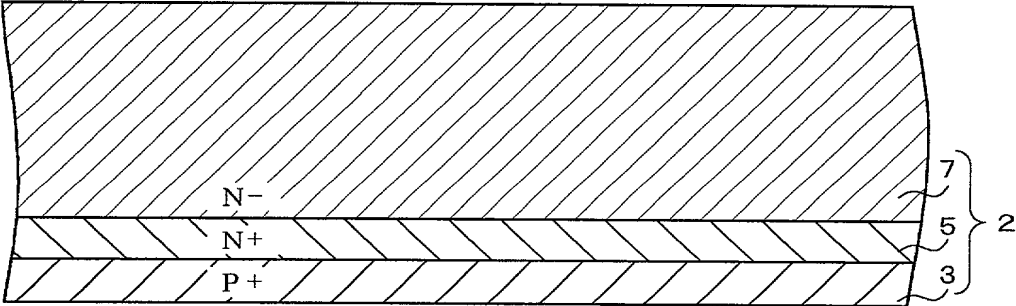


FIG.4B

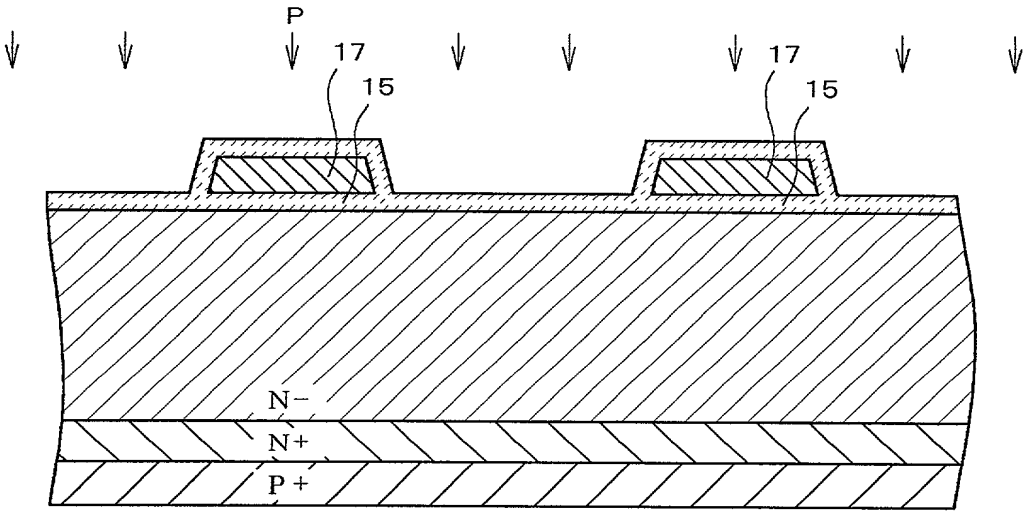


FIG.4C

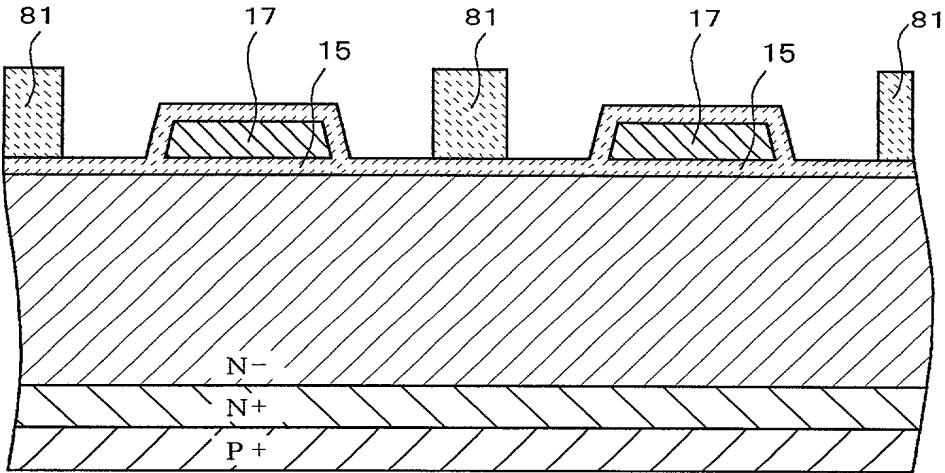


FIG.5A

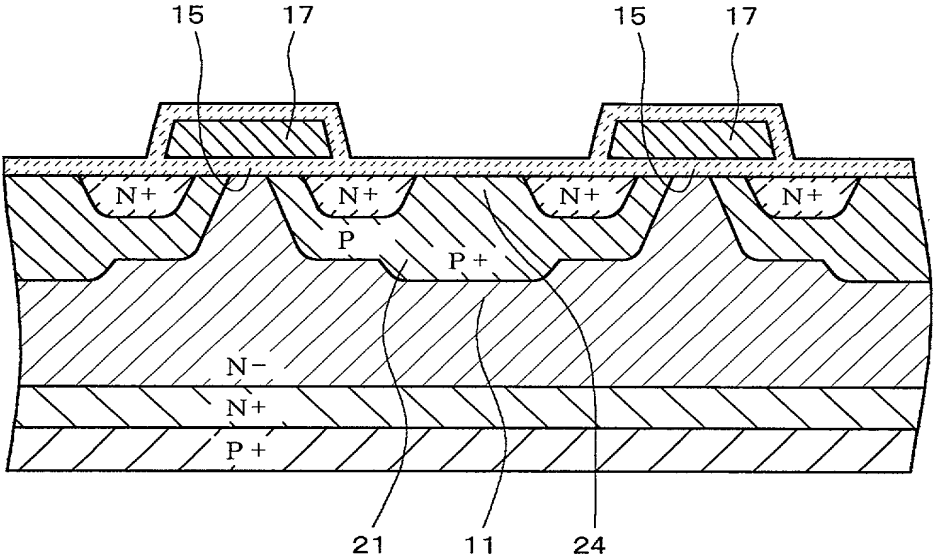


FIG.5B

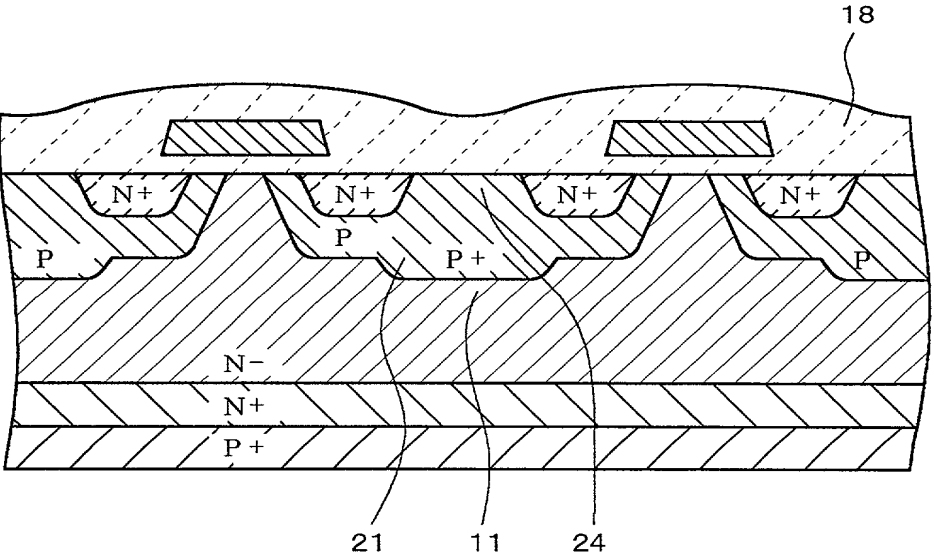


FIG.6A

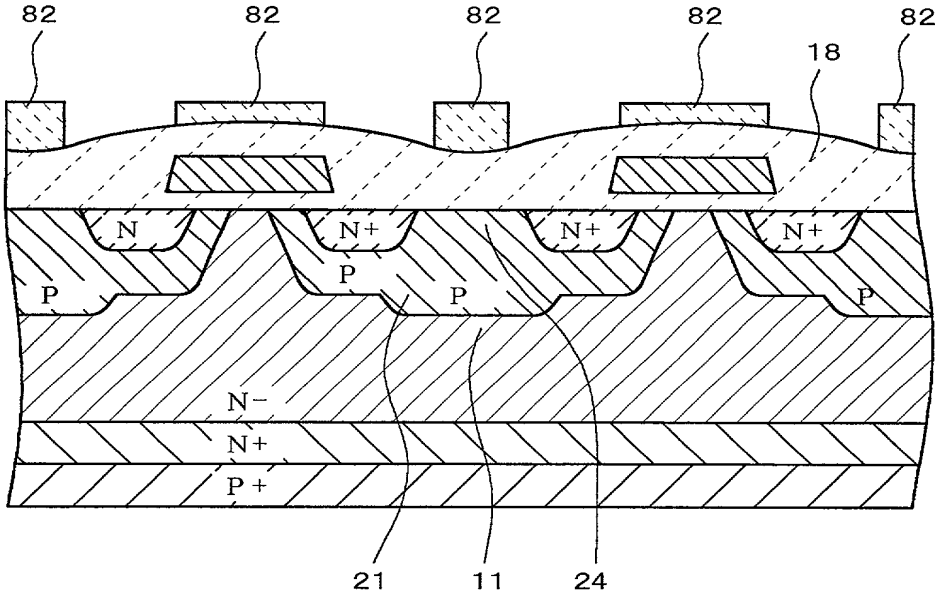


FIG.6B

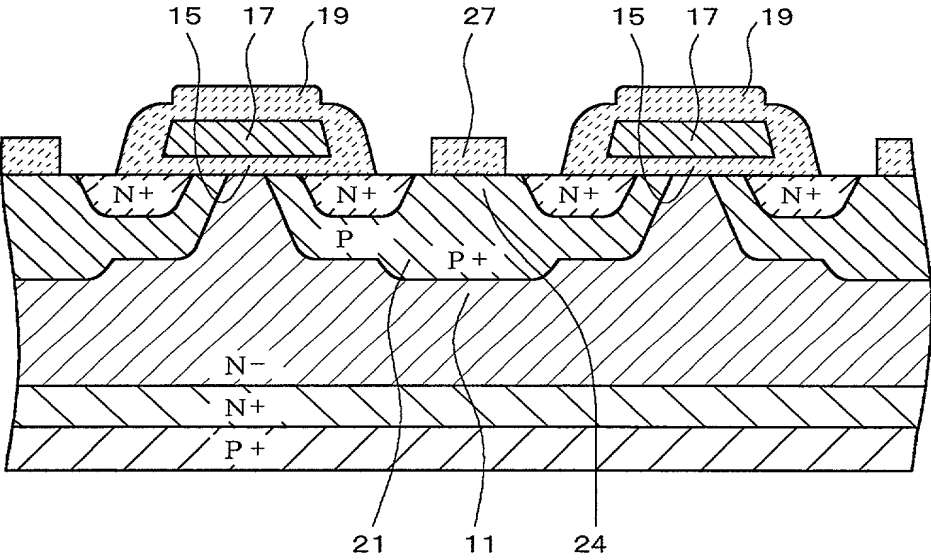


FIG.7A

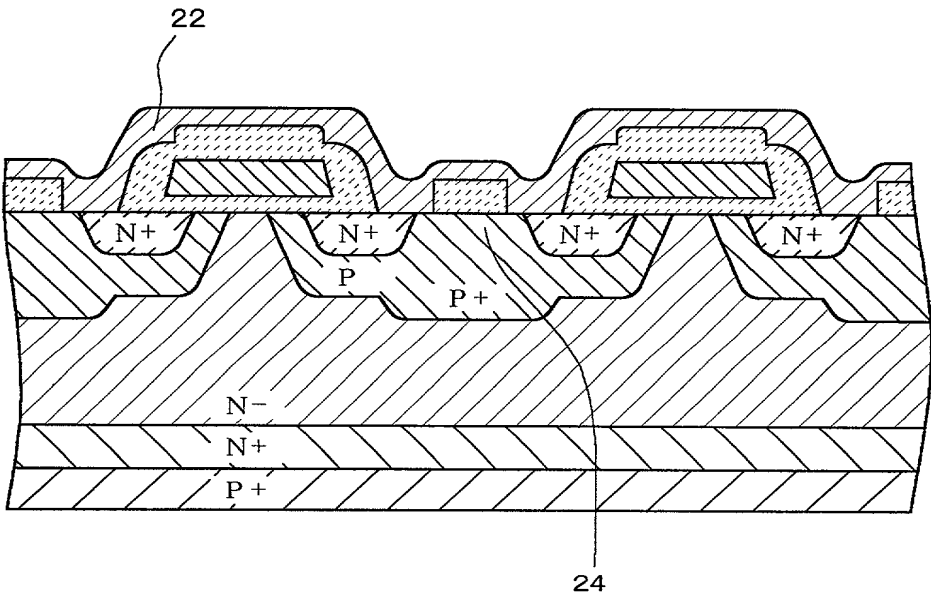


FIG.7B

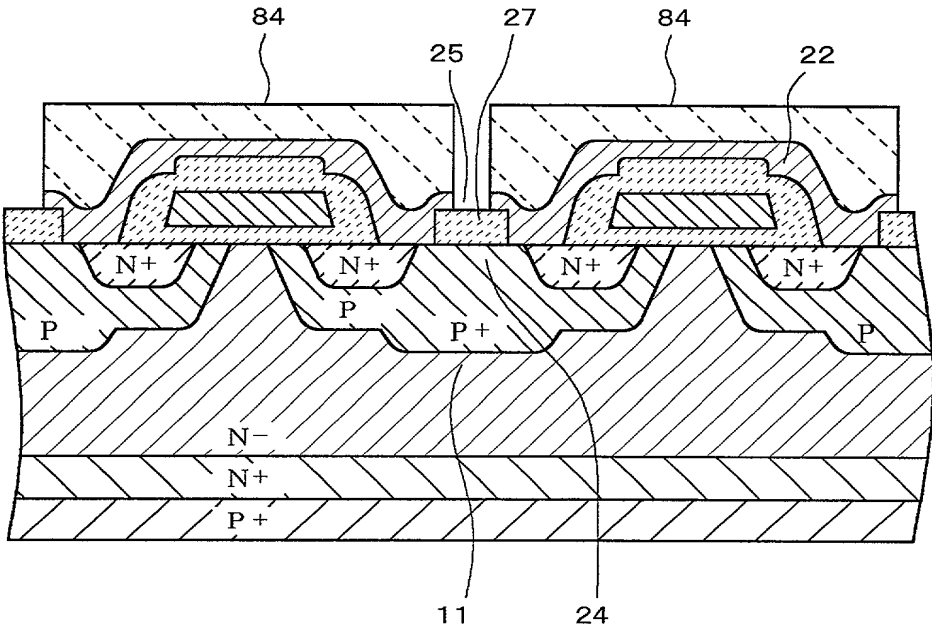
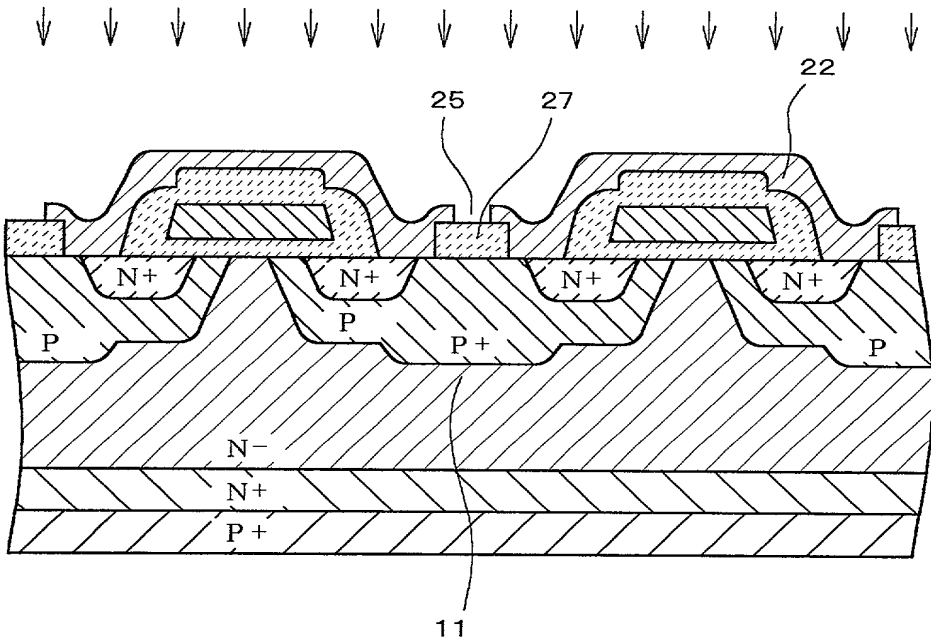


FIG.8



**FIG.9**

**<PRIOR ART>**

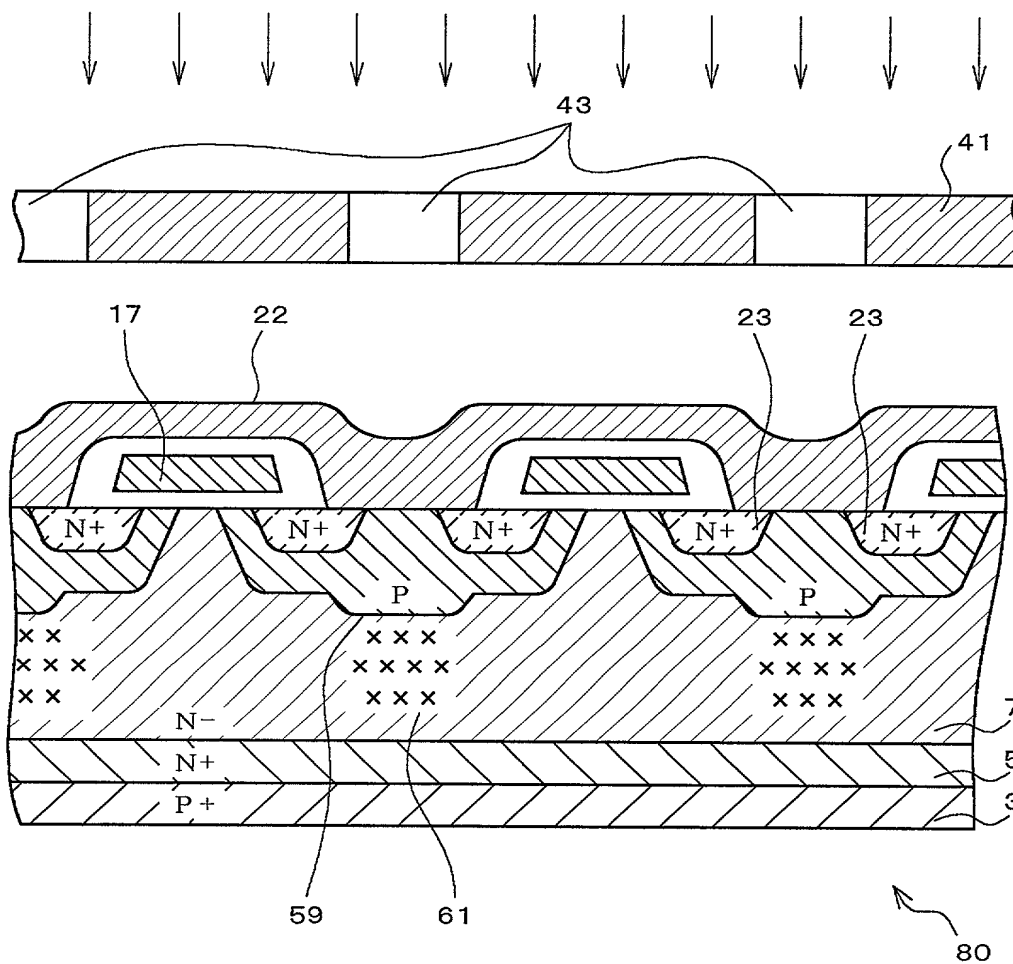
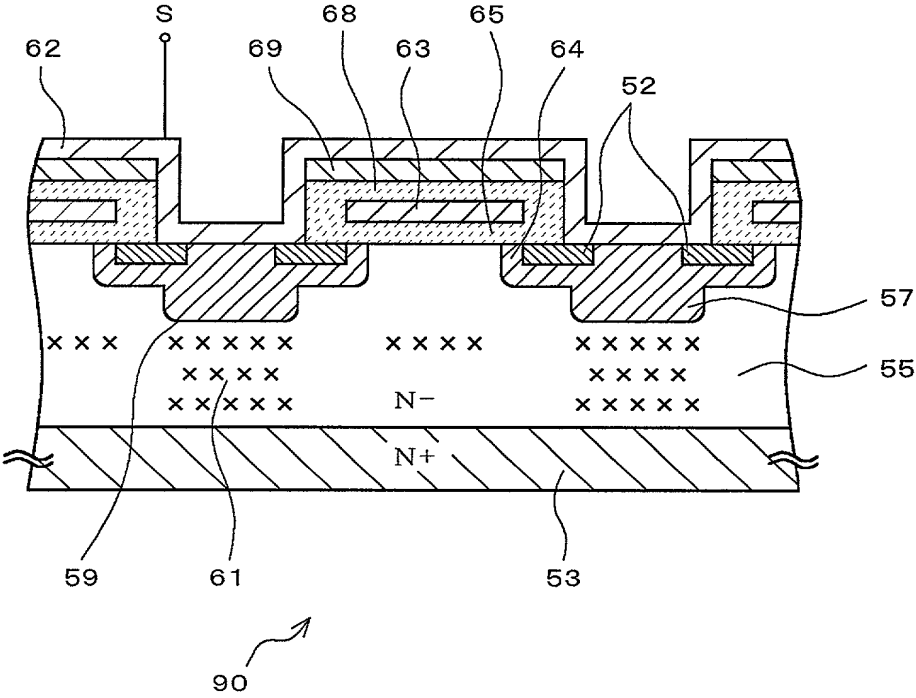


FIG.10

<PRIOR ART>



## United States Patent Application

## COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SEMICONDUCTOR DEVICE AND A METHOD FOR MANUFACTURING THEREFOR

The specification of which

- a. ☒ is attached hereto  
b. ☐ was filed on \_\_\_\_\_ as application serial no. \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. \_\_\_\_\_ filed \_\_\_\_\_ and as amended on \_\_\_\_\_ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☐ no such applications have been filed.  
b. ☒ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
Japan	9-71056	March 25, 1997	
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)
PCT/JP98/01325	March 25, 1998	Pending

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)

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Please direct all correspondence in this case to Merchant, Gould, Smith, Edell, Welter & Schmidt at the address indicated below:

Merchant, Gould, Smith, Edell,  
Welter & Schmidt  
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90 South Seventh Street  
Minneapolis, MN 55402-4131

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2  0  1	<b>Full Name Of Inventor</b>	<b>Family Name</b> SAKAMOTO	<b>First Given Name</b> Kazuhisa	<b>Second Given Name</b>
	<b>Residence &amp; Citizenship</b>	<b>City</b> Kyoto	<b>State or Foreign Country</b> Japan	<b>Country of Citizenship</b> Japan
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<b>Signature of Inventor 201:</b>				<b>Date:</b>

## § 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)–(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim;
- (2) It refutes, or is inconsistent with, a position the applicant takes in:
  - (i) Opposing an argument of unpatentability relied on by the Office, or
  - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application:
- (2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.